

RTP SHALLOW JUNCTION FORMATION OF LOW ENERGY BORON IMPLANTS INTO PREAMORPHIZED SILICON

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The formation of shallow junctions by rapid thermal processing (RTP) of 10 and 20 keV boron implants into both single crystal and preamorphized silicon wafers is investigated. Dopant activation and junction depths are studied over a wide range of anneal temperatures and times in preamorphized silicon. A two step anneal consisting of a low temperature (550°C) furnace anneal and a higher temperature RTP anneal is compared to a one step RTP anneal for junction depth and uniformity. Junction depths of less than 1200 Å and sheet resistances of 100 Ω/□ were achieved for 10 keV, 1.2E15 ions/cm² boron implants. The use of spreading resistance probe as an analytical tool to determine amorphous layer thickness is also discussed.

1. Introduction

The reduction in lateral dimension required to achieve the increased demand on VLSI devices, necessitates a corresponding scale down of junction depths. These junctions must have relatively low sheet resistivities (e.g. 100 Ω/□) as well as excellent uniformities across wafers up to 200 mm diameter. The most difficult shallow junctions to form are boron doped junctions of low resistivity (for p+ source-drain regions). This is a result of boron's high channeling probability for low energy implantation and its high diffusivity during annealing.

Workers [1-8] have used many combinations of implantation and annealing procedures to come up with an optimum technique for shallow p+ junction formation. Techniques vary from regular furnace anneals with very low energy BF₂⁺ and B⁺ implants into preamorphized substrates [1,2]; BF₂⁺ into single crystal Si substrates [3,4] and B⁺ implants with optimized wafer orientations [5]; rapid thermal processing (RTP) anneals with preamorphized and single crystal substrates [6]; and two step anneal [7] of preamorphized wafers involving a furnace for the first step and a RTP anneal for the second step. Electron beam annealing has also been used for the formation of shallow junctions [8].

This paper reports on various procedures for forming shallow p+ junctions. This study investigates the effects of preamorphization, one step versus two step anneals, and wafer orientation for implants into single crystal silicon. All implants are with boron of 10 and 20 keV. The relationship between junction depth and dose for a fixed RTP anneal cycle for shallow junctions of usable sheet resistivities is experimentally determined. Some uniformity benefits of a two step anneal over one step anneal are discussed. Data used to determine preamorphization depths across a wafer are also presented.

2. Experimental

All implants were on (100), 2 Ω cm, 100 mm diameter n-type bare silicon substrates. The preamorphization was achieved by a two step ²⁸Si⁺ implant of 150 keV, 2E15 ions/cm² followed by 50 keV, 2E15 ions/cm² implant using a Varian 160-10 high current implanter. This preamorphization implant was an optimization of earlier work [9] and gave an amorphous region of 0.4 μm width as measured by TEM [10]. An empirical measure of the amorphous region depth is given by spreading resistance probe (SRP) measurements across a test wafer. The preamorphization energies were chosen so that the entire B⁺ implant be within the amorphous region.

The boron implants were performed on preamorphized substrates and single crystal substrates. The single crystal substrates were either oriented at 0° or 45° twist angle to the horizontal scan. Energies were either 10 or 20 keV and the doses ranged from 4E14 to 2.4E15. All boron implants were performed in a Varian 350D serial implanter at a tilt angle of 7°.

Two types of anneals were studied. The first type was a one step RTP anneal in a Varian RTP-800 lamp array system at different conditions ranging from 1000 to 1200°C end point temperatures and for times from 1 to 5 s in an N₂ ambient. The second type of anneal was a two step anneal involving a 550°C, 2 h furnace anneal to anneal out the damage, followed by a RTP anneal for activation.

Dopant profiles and junction depths were obtained by SRP analysis at the center point of the wafer, and uniformities across the wafer were determined by four point probe measurements on a Prometrix Omniprobe unit.

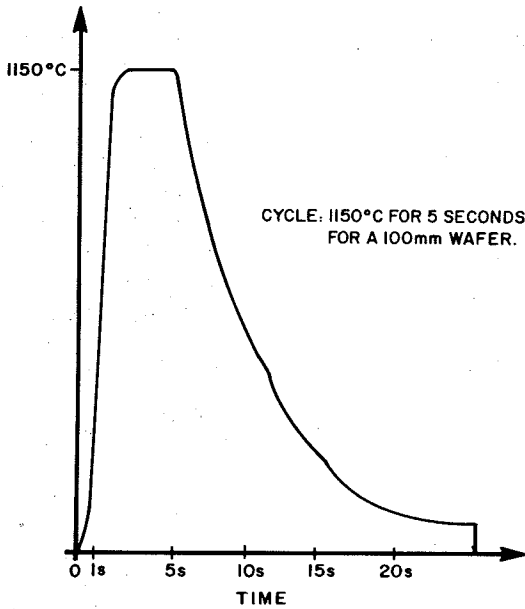


Fig. 1. RTP-800 time-temperature profile for a 1150°C, 5 s anneal with a 100 mm wafer.

3. Results

Many of the RTP anneals were done at fixed time (5 s) and temperature (1150°C). Fig. 1 illustrates this time-temperature profile. The junction depth versus dose into preamorphized silicon for this fixed time-temperature RTP anneal is given in fig. 2. The effects of channeling for boron 6E14 ions/cm², 20 keV implant into preamorphized and single crystal silicon oriented at 0° and 45° is shown in fig. 3. This plot shows that 45° orientation on a silicon wafer helps but

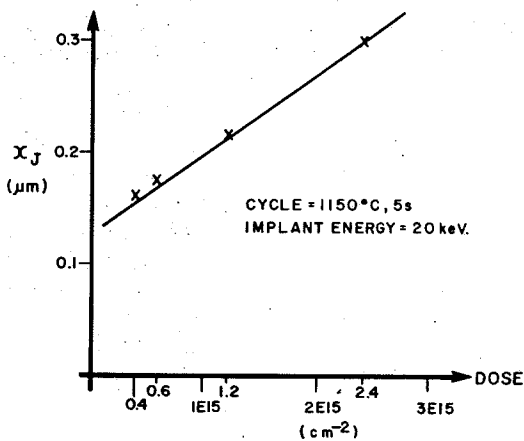


Fig. 2. Junction depth by SRP versus implanted B⁺ dose into preamorphized silicon; for fixed 1150°C, 5 s RTP anneal cycles.

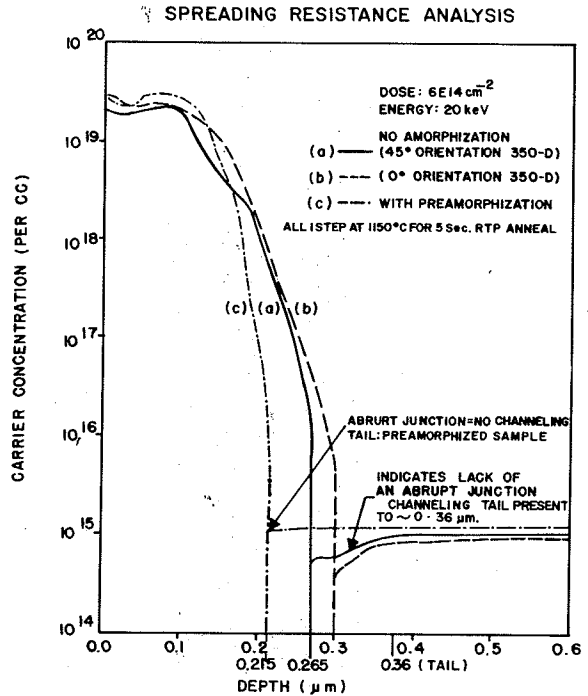


Fig. 3. Junction depths in single crystal silicon with implant orientations of 0° and 45° twist angle, and in preamorphized silicon. All implants are B⁺, 6E14, 10 keV annealed at 1150°C for 5 s by RTP. Carrier concentration profiles are by SRP.

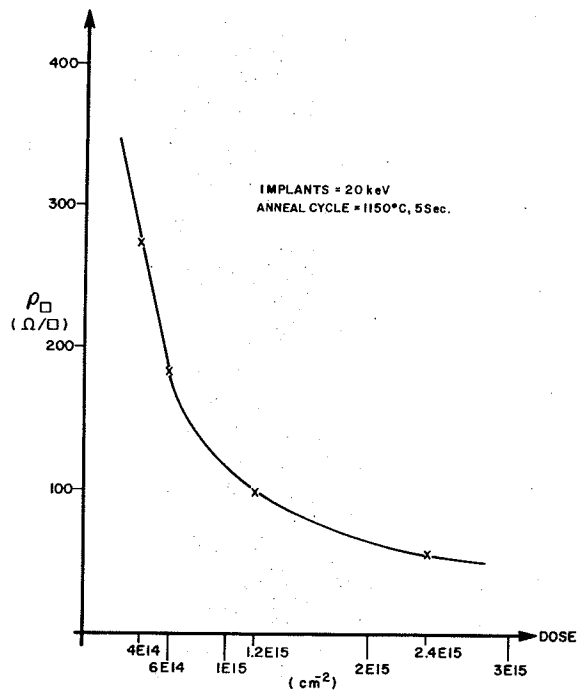


Fig. 4. Sheet resistance versus dose of 20 keV implants for a fixed RTP anneal cycle of 1150°C for 5 s.

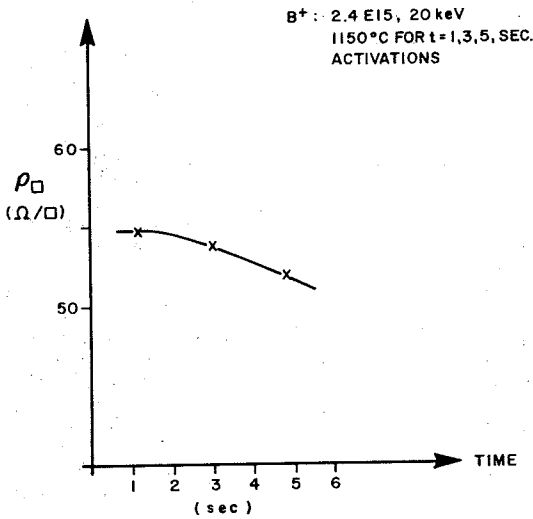


Fig. 5. Sheet resistance versus RTP anneal times at 1150°C for $2.4E15, 20 \text{ keV } B^+$ implants.

the randomizing effects of the amorphous layer is required to minimize channeling. This result is in agreement with earlier work done by others [1].

Fig. 4 shows how the sheet resistivity decreases with dose for a 20 keV implant into preamorphized silicon.

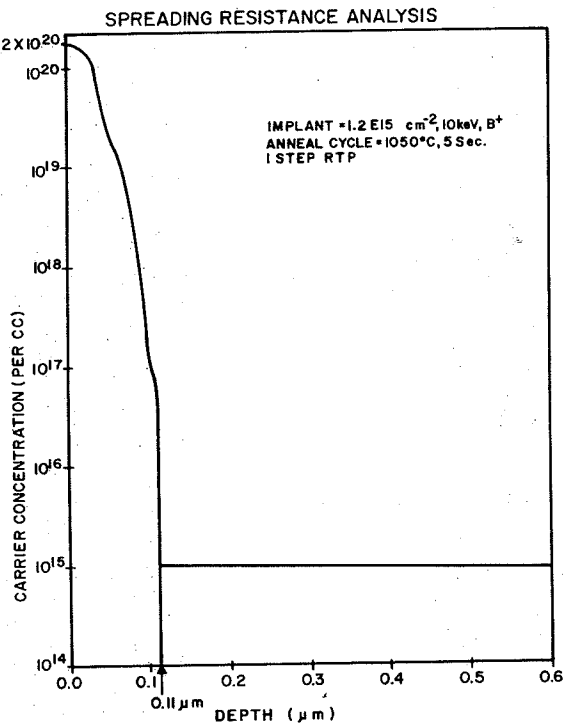


Fig. 6. Carrier concentration profile for $1.2E15, 20 \text{ keV}$ implanted into preamorphized silicon annealed by a one step $1050^\circ\text{C}, 5 \text{ s}$ RTP anneal. These are typically the most shallow junction depths with a sheet resistivity of $100 \Omega/\square$.

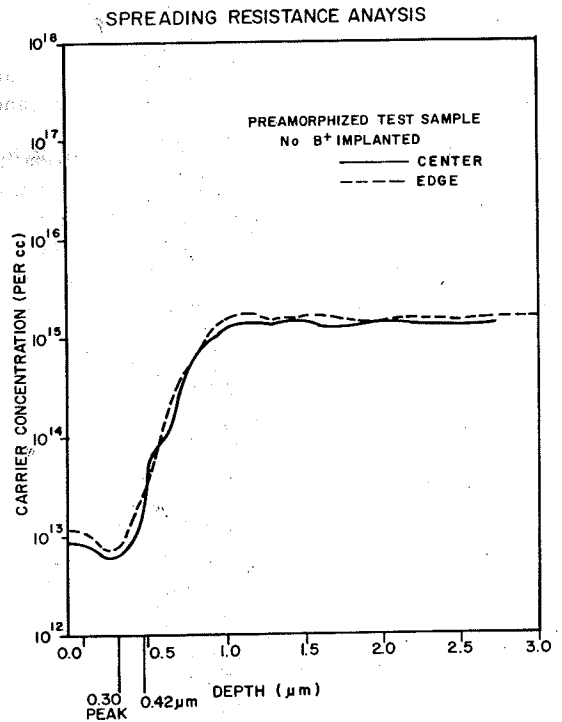


Fig. 7. Spreading resistance profiles of a preamorphized test wafer prior to boron implantation. Profiles taken at center and 0.5 in. from edge of wafer.

These wafers were RTP annealed at 1150°C for 5 s . The sheet resistivity of a $2.4E15$ implant for various RTP anneal times at 1150°C is shown in fig. 5. Currently, lower temperature anneal cycles are being investigated. In addition, the one step and the two step anneals were investigated for both 10 and 20 keV implants of $4E14$ and $6E14 \text{ ions/cm}^2$. In some cases the two step anneals gave better sheet resistance uniformities of 0.5 to 0.8% versus 0.5 to 1.5% for the one step anneals. To within experimental error the junction depths as determined by SRP were equivalent but the average sheet resistivity was 1 to 2% higher for the two step anneal.

An SRP profile of a one step RTP anneal (1050°C for 5 s) of a $1.2E15 \text{ ions/cm}^2, 10 \text{ keV } B^+$ implant is shown in fig. 6. The observed junction depth was 1100 \AA and the measured sheet resistance was about $100 \Omega/\square$. The effective carrier concentration versus junction depth as determined by SRP for a preamorphized sample (center versus edge) is illustrated in fig. 7.

4. Discussion

Since SRP is an electrical measurement of resistance and the sample is an unimplanted uniformly bulk doped preamorphized wafer, it can be argued that the abrupt

increase in carrier concentration (fig. 7) is mostly a result of the mobility increase as the undamaged bulk lattice is approached. This then can be used as an indication of the thickness of the amorphous layer (and a measure of the degree of crystalline damage).

High activation with minimal redistribution from the as implanted profile [1,8] and good uniformity results are achieved with one step RTP anneals. The uniformity for one batch of wafers was more consistent for the two step process. This may be attributed to the nonuniformity of the amount of damage produced by the preamorphization implant and the subsequent more uniform or more complete repair by an extended low temperature (nondiffusing) anneal.

5. Conclusion

Shallow junctions of less than 1200 Å with a sheet resistance of around 100 Ω/\square were obtained with 10 keV boron implants into preamorphized silicon and annealed by one step RTP. Optimized wafer orientation for B⁺ implants followed by RTP anneal is insufficient to give shallow junctions in single crystal silicon with the boron energies and doses used. A preamorphized layer is required to minimize the channeling and RTP is required to give high activation with minimal dopant redistribution. Two step anneals give more consistent uniformities than one step anneals.

Empirical measurements using SRP to determine preamorphization implant layer thicknesses are in agree-

ment with the shallow junctions obtained and with previous TEM measurements.

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